Raghavendra Pradyumna Pothukuchi

Yale University

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Research

Quantum, Cognition and Computing Systems: Enabling a Novel and Virtuous Research Cycle

PhD Dissertation: **Intelligent Systems for Efficiency and Security**

Primary area: Computer architecture and systems
Secondary areas: Quantum computing, Cognitive neuroscience, Formal control, Energy and power efficiency, Security, Machine learning, Datacenters and cloud, Compilers

Education

Yale University *2021–Current*
Associate Research Scientist
Mentor: Abhishek Bhattacharjee

University of Illinois at Urbana-Champaign (UIUC) *2020*
Ph.D. in Computer Science (CS)
Advisor: Josep Torrellas

University of Illinois at Urbana-Champaign *2014*
M.S. in Computer Science 3.96/4.00

Birla Institute of Technology & Science, Pilani *2011*
B.E. (Hons.) Electrical and Electronics Engineering (EEE) 10.00/10.00

Honors and Awards

- **CRA NSF Computing Innovation Fellow (CI Fellow)**, *one of the 69 researchers across USA awarded by the Computing Research Association (CRA) and National Science Foundation (NSF),* 2021-2023
  Press release: https://cccblog.org/2021/07/22/announcing-the-2021-computing-innovation-fellows/
- **Swati and Mukul Chawla Scholarship,** *Parallaxes Capital, UIUC,* 2020
- **Cover feature,** *IEEE Control Systems,* 2020
- **IEEE Computer Society Lance Stafford Larson Paper Award,** *2nd prize* (2019) *and 3rd prize* (2018)
- **W. J. Poppelbaum Award** *for architecture design creativity, Dept. of CS, UIUC,* 2018
- **Rising Stars in Computer Architecture** *for being one of the top candidates in the field, Georgia Institute of Technology,* 2018
- **Mavis Future Faculty Fellow,** *College of Engineering, UIUC,* 2017
- **ACM Student Research Competition winner,** *PACT (International conference on Parallel Architectures*

and Compilation Techniques), 2017

- **Certificate in Foundations of Teaching,** *Center for Innovation in Teaching and Learning, UIUC,* 2017
- **Best Paper Award nominee,** *PACT,* 2017
- **Best Graduating Student,** *Prof. L. K. Maheshwari foundation, BITS Pilani,* 2011
- **University Gold Medal** *for outstanding academic achievement, BITS Pilani,* 2011
- **GE Innovation Award,** *John F. Welch Technology Centre, General Electric (GE),* 2010
- **University Merit Scholarship,** *BITS Pilani,* 2007 – 2011

Industry Experience

AMD Research, Austin, USA **Mar'18–May'18, May'17–Dec'17**

Coop Intern

- Developed a modular composable resource control network for heterogeneous computers
- Prototyped the proposed design on a 2 CPU-GPU node
- Filed for a patent and authored a paper that was accepted at MICRO 2019

Nvidia Graphics, Bangalore, India **Aug'11–Jun'12**

ASIC Design Engineer

- Closed timing in multiple chips at 28 nm technology
- Analyzed USB 2.0 IO modules in Tegra 4 mobile SoC, high-speed memory interface paths in Tesla GPGPU for high performance computing and Kepler GPU for desktop graphics

Nvidia Graphics, Bangalore, India **Spring'11**

Hardware Design Intern

- Developed a SPICE based timing analysis framework of multi-voltage IO paths in Nvidia's first 28 nm GPU

Indira Gandhi Center for Atomic Research, Kalpakkam, India **Summer'09**

Research Intern

- Developed a micrometer positioner read-out using a Programmable System on Chip (PSoC) based embedded system, and LabVIEW virtual instrumentation

Tutorial Organization

R. P. Pothukuchi, H. Hoffmann, K. Rao, J. Torrellas, **"Combining Machine Learning and Control Theory for Computer Architecture (MCAt)"**, *held at the International Symposium on Microarchitecture* (**MICRO**), 2019. http://iacoma.cs.uiuc.edu/mcat/index.html [55 participants]

Publication Record

7 conferences (3 ISCA, 1 MICRO, 1 PACT, 1 CDC, 1 CGO), 1 manuscript, 1 journal (CSM), 2 technical reports, 2 poster papers, and 1 patent.

131 citations (https://scholar.google.com/citations?user=WXYEFn4AAAAJ&hl=en)

Conferences

» H. Nam, R.P. Pothukuchi, B. Li, N. S. Kim, J. Torrellas, **"Microarchitecting an Adversarial Machine Learning Model to Defend Against Side-channel Attacks"**, *submitted*, 2021.

» J. Vesely*, R. P. Pothukuchi*, K. Joshi, S. Gupta, J. D. Cohen, A. Bhattacharjee, **"Distill: Domain-Specific Compilation for Cognitive Models"**, *International Symposium on Code Generation and Optimization* (**CGO**), April 2022. [29% acceptance]
*Joint first authors

» R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, A. Schwing, J. Torrellas, **"Maya: Using Formal Control to Obfuscate Power Side Channels"**, *International Symposium on Computer Architecture* (**ISCA**), June 2021. [19% acceptance]

» R. P. Pothukuchi, J. Greathouse, K. Rao, L. Piga, C. Erb, P. Voulgaris, J. Torrellas, **"Tangram: Integrated Control of Heterogeneous Computers"**, *International Symposium on Microarchitecture* (**MICRO**), October 2019. [23% acceptance] **2nd prize, IEEE Computer Society Lance Stafford Larson paper award**

» R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas, **"Modular Computer Resource Management with Multiple Structured Singular Value Controllers"**, *IEEE Conference on Decision and Control* (**CDC**), December 2018. [60% acceptance]

» R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas, **"Yukta: Multilayer Resource Controllers to Maximize Efficiency"**, *International Symposium on Computer Architecture* (**ISCA**), June 2018. [17% acceptance]

» R. P. Pothukuchi, A. Ansari, B. Gopireddy, J. Torrellas, **"Sthira: Systematically Controlling the Error Rates in Variation-Prone Networks-on-Chip for Energy Efficiency"**, *International conference on Parallel Architectures and Compilation Techniques* (**PACT**), September 2017. [23% acceptance] **Best paper nominee**

» R. P. Pothukuchi, A. Ansari, P. Voulgaris and J. Torrellas, **"Using Multiple Input, Multiple Output Formal Control to Maximize Resource Efficiency in Architectures"**, *International Symposium on Computer Architecture* (**ISCA**), June 2016. [20% acceptance] **3rd prize, IEEE Computer Society Lance Stafford Larson paper award**

Journals

» R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas, **"Control Systems for Computer Systems: Making Computers Efficient with Modular, Coordinated and Robust Control"**, *IEEE Control Systems* (**CSM**), March 2020. [Impact factor 6.228] **Cover Feature**

Patents

» R. P. Pothukuchi, J. Greathouse, L. Piga, **"Distributed Multi-Input Multi-Output Control Theoretic Method to Manage Heterogeneous Systems"**, *US Patent 10,928,789,* 2021.

Tech Reports

» R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas, **"Designing a Robust Controller for Obfuscating a Computer's Power"**, *Technical Report,* [Online] http://iacoma.cs.uiuc.edu/iacoma-papers/

isca21_1_tr.pdf, June 2021.

» R. P. Pothukuchi, J. Torrellas, **"A Guide to Design MIMO Controllers for Architectures"**, *Technical Report,* [Online] http://iacoma.cs.uiuc.edu/iacoma-papers/mimoTR.pdf, April 2016.

Posters and Poster Papers

» R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas, **"Multilayer Compute Resource Management with Robust Control Theory"**, *International Conference on Parallel Architectures and Compilation Techniques* (**PACT**), September 2017, **Winner, ACM Student Research Competition**

» Pradyumna, P.R., Tarun, C.K.S., Bhanot, S, **"Remote Experimentation of "No-load Tests on a Transformer" in Electrical Engineering"**, *International Conference on Engineering Education: Innovative Practices and Future Trends* (**AICERA**), July 2012.

Grant Writing Experience

» **"CSR: Medium: Effective Control to Maximize Resource Efficiency in Large Clusters; Hardware, Runtime, and Compiler Perspectives"**, *NSF Award #1763658,*
PIs: Josep Torrellas, Laxmikant Kale, David Padua at UIUC, 2018.
Media coverage: https://dailyillini.com/news/2018/11/01/ui-professors-receive-1-2-million-grant-to-improve-computer-efficiency/

» **"SPX: Secure, Highly-Parallel Training of Deep Neural Networks in the Cloud Using General-Purpose Shared-Memory Platforms"**, *NSF Award #1725734,*
PIs: Josep Torrellas, Christopher Fletcher at UIUC, 2017.

Invited Talks

Intelligent Systems for Extreme-Efficiency and Security

» Georgia Institute of Technology, February 2021

» University of California at Los Angeles, February 2020

» Pennsylvania State University, February 2020

» Yale University, November 2019

Maya: Using Formal Control to Obfuscate Power Side-channels

» Intel Side Channel Academic Program, Workshop, Intel, May 2021

» Security and Privacy Research at Illinois (SPRAI), UIUC, September 2019

Extreme-Efficiency Computing

» Indian Institute of Sciences (IISc), Bengaluru, India, January 2019

» Intel Research, Bengaluru, India, January 2019

» Indian Institute of Technology (IIT), Delhi, India, January 2019

» Rising Stars in Computer Architecture Workshop, Georgia Tech, September 2018

Teaching & Mentoring

At UIUC: Mentored 2 graduate students (Masters) and 1 undergraduate.
At Yale: Mentored 2 undergraduates. Currently mentoring 2 graduate students (PhD) and 13 undergraduates.

Mentoring

Research Mentor **Sep'20–Curr.**

Yale University

» Mentoring a graduate student on systems for Brain-Computer Interfaces, and another student on brain-inspired memory system design for computers.

» Mentoring undergraduates on research projects in quantum computing, cognitive science and systems

» 5 undergraduates are working on quantum implementations of cognitive models

» 8 undergraduates are working on deploying cognitive models on resource-constrained hardware

Mavis Mentor **Aug'16–Aug'17**

College of Engineering, UIUC

» Mentored two graduate students and supported the research towards their master's degree

MUSE Mentor **Aug'16–Aug'17**

College of Engineering, UIUC

MUSE: Mentoring Undergraduate Students in Engineering

» Mentored a sophomore by defining the scope, goals and guiding progress in an introductory machine learning research project

Teaching

Parallel Computer Architecture **Spring'17**

Teaching Assistant, UIUC

CS 533: Graduate course on advanced architecture topics (19 students)

» Taught three lectures, created and graded homeworks, organized office hours

Energy Efficient Computer Architecture **Fall'16**

Teaching Assistant, UIUC

CS 598: Discussion course on recent ideas for energy efficient architectures (10 students)

» Moderated and provided insights on discussions during four lecture sessions

Computer System Organization **Fall'15**

Teaching Assistant, UIUC

CS 433: Early graduate/senior course on computer architecture (25 students)

» Taught two lectures, designed homeworks and examinations, and organized office hours

Microelectronic Circuits **Fall'10**

Teaching Assistant, BITS Pilani

Course on the analysis and design of analog MOS circuits (~80 students)

» Led micro-teaching classes, and laboratory sessions on Cadence Virtuoso and Eldospice tools

Engineering Graphics **Fall'08**

Teaching Assistant, BITS Pilani

Course on introductory computer aided drawing (~120 students)

» Developed AutoCAD laboratory modules and organized lab hours

Service

Peer reviewing

22 manuscripts

» **Journals:** IEEE Transactions on Computers (TC), ACM Transactions on Internet of Things (TIOT), IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS), IEEE Micro, IEEE Computer Architecture Letters (CAL), Elsevier Journal of Parallel and Distributed Computing (JPDC), Wiley Interdisciplinary Reviews (WIREs): Data Mining and Knowledge Discovery

» **Conferences:** ISCA'22, IPDPS' 21

» **Conferences (through Prof. Josep Torrellas):** ISCA, HPCA, MICRO, ASPLOS, PACT

Professional Memberships

» ACM, IEEE (IEEE Computer Society and IEEE Control Systems Society), AAAS

Organizational Service

Computer Architecture Student Association (CASA) **2020–Curr.**

Co-founder

https://www.comparchsa.org/

» CASA's vision is to promote student wellbeing and a sense of belonging in the computer architecture community

» Worked with SIGARCH and TCCA to establish CASA

» The original proposal is available at: http://ieeetcca.org/wp-content/uploads/2020/05/Arch_student_wellbeing_27MAY.pdf

Students Advising on Graduate Education (SAGE) Board **Aug'17–Aug'18**

Graduate College, UIUC

» Advisory member to the Dean on matters related to graduate affairs

Engineering Graduate Student Advisory Committee (EGSAC) **Aug'16–Aug'17**

College of Engineering, UIUC

» Advisory member to the Dean, College of Engineering

» Proposed an interdisciplinary fellowship program, events to promote interdisciplinary engagement, and improve student wellness

Computer Science Graduate Academic Council (CSGAC) **Aug'15–Aug'17**

Dept. of CS, UIUC

» Advisory member to the department on improving graduate academics

» Supported departmental activities and served as a liaison between CSGAC and EGSAC

» Interacted as area representative with prospective students on campus visits

Architecture Reading Group **Aug'15–Aug'17**

Dept. of CS, UIUC

» Co-organized the weekly reading group on computer architecture papers

References

Josep Torrellas
Saburo Muroga Professor, Dept. of CS, UIUC
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Wen-mei Hwu
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